IN THE SPECIFICATION

Please amend the paragraph beginning on page 8, line 14, of the specification as follows:

The design and operation of the digital preliminary stage 50 is explained in more detail below. Its design is shown in the block diagram in the left-hand part of Figure 2. The signal coming from the equalizer 40 is first rectified in a rectifier 51. The rectified signal is then supplied to a delay stage 52. The delay stage 52 delays the data signal by one sampling clock period. The delayed signal is supplied to a b input of a subtraction stage ~~51~~ 53. The input of the subtraction stage 53 is supplied with the undelayed data signal. In the subtraction stage 53, the delayed sample at the b input is deducted from the undelayed, current sample at the input. The resulting differential value is then analysed in a processing stage 54. In the simplest case, the processing stage 54 assigns one of three possible output values to the differential value. Specifically, in the simplest case, these are the output values +1, 0, -1. In this context, assignment proceeds as follows: it comprises a simple mathematical sign check. If the differential value is greater than 0, then the value +1 is assigned to it. If the differential value is 0 within the bounds of computational accuracy, then the value 0 is assigned to the differential value. If the differential value is less than 0, then the value -1 is assigned to it as output value.